Gp 2823

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#9/IDS
12-9-02
V Short

In re application of

Ryo KUBOTO, et al.

Docket No: Q62494

Appln. No.: 09/817,233

Group Art Unit: 2823

Confirmation No.: 8072

Examiner: Hsien Ming LEE

Filed: March 27, 2001

For: MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE HAVING DRAM CAPACITORS

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached PTO/SB/08 A & B (modified) form and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

1. Japanese Unexamined Patent Application No. 7-66295, published March 10, 1995.

2. Japanese Unexamined Patent Application No. 11-307740, published November 5, 1999.

3. Japanese Unexamined Patent Application No. 11-186521, published July 9, 1999.

4. Japanese Unexamined Patent Application No. 11-186524, published July 9, 1999.

One copy of each of the listed documents is submitted herewith.

The present Information Disclosure Statement is being filed after the later of three months from the application's filing date and the mailing date of the first Office Action on the merits, but before a Final Office Action, Notice of Allowance, or an action that otherwise closes prosecution in the application (whichever is earlier), and therefore Applicant is filing concurrently herewith a Statement Under 37 C.F.R. § 1.97(e). No fee under 37 C.F.R. § 1.17(p) is required.

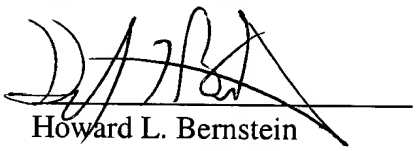
The present Information Disclosure Statement is being filed thirty days or fewer from the communication from a foreign patent office and a Statement Under 37 C.F.R. §1.704(d) is attached.

In compliance with the concise explanation requirement under 37 C.F.R. § 1.98(a)(3) for foreign language documents, Applicant encloses herewith a copy of a Communication from the Japanese Patent Office dated November 6, 2002 in a counterpart application citing such documents, together with an English-language version of that pertinent portion indicating the degree of relevance found by the foreign patent office.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application.

Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

Respectfully submitted,



Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: December 4, 2002

Ref Q62494

Transmission date: November 6th, 2002

Record (Refer to the List of Cited Literature, etc. for the cited literature.)

- Claims 1 to 3
- Reason A
- Cited Literature 1, 2, 3, and 4
- Remarks

Described in Cited Literature 1 is a semiconductor device and manufacturing method thereof wherein, after forming transistors of a DRAM unit and a peripheral circuit region (logical circuit), a film between layers is formed, and after forming groves in said film between layers and forming a polysilicon film that has HSG formed over the entire surface, the aforementioned polysilicon film is removed except for from said groove region (Specifically, refer to Figs. 21 to 24 and the description of the diagrams.)

Described in Cited Literature 2 is a semiconductor device and manufacturing method thereof wherein a DRAM unit and a CMOS logic circuit unit are mix mounted. (Specifically, refer to Figs. 5 to 10 and the explanation of the diagrams.)

Described in Cited Literature 3 is the use of BPSG in a film between layers. (Specifically, refer to sections {0042} to {0045}, Fig. 7, and the explanation of the diagrams.)

Described in Cited Literature 4 is the fact that the gate electrode of a p-channel transistor of a CMOS circuit unit is made into the p-type. (Specifically, refer to Fig. 7 and the explanation of the diagrams.)

List of Cited Literature, etc.

1. Japanese Unexamined Patent Application Publication No. H11-186524
2. Japanese Unexamined Patent Application Publication No. H11-186521
3. Japanese Unexamined Patent Application Publication No. H11-307740
4. Japanese Unexamined Patent Application Publication No. H07-066295

Record of Prior Art Literature Search Results

- Searched fields IPC 7th Edition H01L27/10
  H01L27/108
  H01L27/092
  H01L21/8242
  H01L21/8238

This record of prior art literature search results does not constitute a reason for rejection.